VPX56H2-6 6U VPX AC/DC Power Supply

1,400-Watt Ruggedized, Programmable Power Supply Plug-in Module, Conduction-Cooled, Five Outputs

Made in the USA
Certified Small Business

Description

NAI's VPX56H2-6 is a 1,400-Watt AC/DC Power Supply that plugs directly into a standard 6U VPX chassis with a VITA 62 1.0" power supply slot. This off-the-shelf solution for VITA 46.0 and VITA 65 systems is compatible with VPX specifications; supports all VITA standard I/O, signals, and features; and conforms to the VITA 62 mechanical and electrical requirements for modular power supplies.

The VPX56H2-6 programmable power supply is conduction-cooled through the card edge/wedgelock. It accepts 3Ø AC or +270 VDC input and provides five outputs and I/O at up to 1,400 Watts.

The VPX56H2-6 supports a variety of standard features, including continuous Background Built-in-Test (BIT); remote error sensing and protection against transients, over-voltage, over-current, and short circuits. With its intelligent design, the VPX56H2-6 also has the flexibility to address special needs. Features include current share and alignment keys for input and output configurations.

This COTS power supply is specifically designed with NAVMAT component derating for rugged defense and industrial applications. It is also designed to meet the many harsh environmental requirements of military applications.

Features

- Ideal for rugged 6U VPX power applications
- Standard VPX-compatible connectors and I/O per VITA 62
- Compatible with System Management Bus per VITA 46.11
- Off-the-shelf solution for VITA 46.0 and VITA 65 systems
- Supports all VITA standard I/O, signals, and features
- Accepts 3Ø AC or +270 VDC input
- Provides five outputs and I/O at up to 1,400 Watts
- "Heavy" +12Vdc Configuration Available
- Continuous Background Built-in-Test (BIT)
- User Programmability
- Current share
- Status LED
- Alignment keys per VITA 62
- Input transient protection per MIL-STD-704F
- Integrated EMI filtering per MIL-STD-461F
- Environmental Performance per MIL-STD-810G and VITA 47
- Operates at full load through the entire -40°C to +85°C temperature range

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Electrical Specifications

AC Input Characteristics	
Input	Accepts 115 VAC (Line-to-Neutral), Three Phase AC, or 270 VDC (see Input Pinout Designations Table, page 9 and Ordering Information, page 9)
Input Voltage Range	±10%
Frequency Range	47 Hz to 440 Hz
EMI/RFI	MIL-STD-461F – CE102, CS101, CS114 a & b, CS116 compliant (requires additional system filtering)
Input Transient Protection	Per MIL-STD-704F
Output Power	1,400 Watts typical at 85 ºC (see Output Power Table, including notes, page 3)
Output Voltage	VPX outputs standard (see Output Power Table, page3)
Efficiency	88% typical
Line Regulation	Within 0.5% or 20 mV (whichever is greater) for low to high line changes at constant load; For current share units: 1.5% for VS1/VS2, VS3; 2% for +3.3 VDC_Aux; 2% for ±12 VDC_Aux
Load Regulation	0.5% or 20 mV (whichever is greater) for 0 to 100% of rated load at nominal input line with remote sense; 1% for -12 VDC_Aux , +12 VDC_Aux; For current share units: 1.5% for VS1/VS2, VS3, +3.3 VDC_Aux; 2% for +12 VDC_Aux
PARD (Noise and Ripple)	1% or 50 mV p-p max per VITA 62; measurements are made with a 20 MHz bandwidth instrument connected on load wires < 5 inches from power supply and terminated with 1uF capacitors across load lines
Load Transient Recovery	Output voltage returns to regulation limits within 0.5 msec, half to full load
Load Transient Under/Overshoot	5% of nominal output voltage set point (0.6 V max)
Short Circuit Protection	Protected for continuous short circuit with automatic recovery
Current Limiting	All outputs 105% to 130%
Over Voltage Protection	Automatic electronic shutdown if outputs exceed 125% ±10%
Remote Error Sensing	Sensing pins compensate for up to 0.5 V drop on VS1 to VS3 & +3.3Vdc_Aux outputs
Isolation Voltage	1000 VDC input to output and input to case; 100 VDC output to case
Insulation Resistance	50 Mega Ohm at 50 VDC

All specifications are subject to change without notice.

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Additional Specifications

Physical/Environmental	
Temperature Range	Operating: -40°C to +85°C at 100% load (temperature measured at card edge, conduction via card edge); Storage: -55°C to +100°C per VITA 47 CC4)
Temperature Coefficient	0.01% per °C
Shock	30 G's each axis per MIL-STD-810G, Method 516.6, Procedure 1; Hammer shock per MIL-S 901; ½ sine wave per VITA 47 OS2
Acceleration	6 G's per MIL-STD-810G, Method 513.6, Procedure II; 14 G's per Procedure 1
Vibration	Per MIL-STD-810G, Method 514.6, Procedure 1A
Humidity	95% at 71°C per MIL-STD-810G, Method 507.5 (non-condensing)
Altitude	1,500 feet below sea level to +60,000 feet above sea level - per VITA 47
Sand/Dust	Per MIL-STD-810G, Method 510.5
Fungus	Per MIL-STD-810G, Method 508.6
ESD	15kV EN61000-4-2 per VITA 47
Enclosure	Aluminum housing to aluminum baseplate
Dimensions	See Mechanical Layout
Finish	Chemical film IAW MIL-DTL-5541, Type II, Class 3
Interface	50 Micro-Inch Gold on contacts; plated tails for tin whisker mitigation; See Connector Part Numbers below
Weight	3.85 lbs. typical

All specifications are subject to change without notice.

Output Power *Note 1

Standard VITA 62 Outputs			Heavy +12Vdc		
Designation	Volts	Amps	Designation	Volts	Amps
VS1/VS2**Note 2	+12.0	80 (Total)	VS1/VS2/VS3***Note 3	+12.0	120
VS3	+5.0	50	3.3 V_Aux	+3.3	20
3.3 V_Aux	+3.3	20			
+12_Aux***	+12	3			
-12_Aux***	-12	3			

* Note 1:Total output power limited to 1,400 Watts
** Note 2: VS1 and VS2 are combined into one output
***Note 3 VS1, VS2 and VS3 are combined into one output

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Connectors

Unit Connector		Backplane Connector (Mate)
Input	P0: TE Connectivity p/n: 2314577-1	J0: TE Connectivity p/n 2314581-1
Output	P1: TE Connectivity p/n 2314578-1	J1: TE Connectivity p/n 2309390-2

Feature & Signal Types

Feature/ Signal	Description
ENABLE*	Turns off all of the output voltages, including 3.3 V_AUX, when signal is High. ENABLE* is pulled Low by using a mechanical switch which connects it to SIGNAL_RETURN. A Logic output can also be used to drive the ENABLE*. Opening the switch would turn off all the outputs; closing the switch or applying the Logic output would enable the outputs to come on depending on the state of INHIBIT*. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with INHIBIT*, this signal determines the output power status of the VPX56H2-6 (see Power Status Table, page 4).
INHIBIT*	Turns off all the output voltages. In most implementations, the signal is expected to leave 3.3 V_AUX on. Pulling INHIBIT* Low turns off VS1/VS2, VS3, and ±12 VDC_Aux outputs. An input of <0.8 VDC is regarded as a Low and an input of >2.0 VDC is regarded as a High. A no-connect is also regarded as a High. Along with ENABLE*, this signal determines the output power status of the VPX56H2-6 (see Power Status Table, page 4).
SYSRESET*	An active low open-collector line driven by the Power Monitor module. Signal ensures a clean, stabilized startup based on monitoring the output voltage levels in accordance with VITA 46.0, paragraph 4.8.11. Timing can be factory customized.
FAIL*	Indicates failure when any outputs are not within specification. Signal complies with VITA 65 for active Low. FAIL* signal is Open Drain. It is expected that there will be a pull-up resistor on the backplane.
Geographical Addressing	As defined in VITA 46
Current Share	Allows multiple power supplies to share system load for VS1/VS2, and VS3 outputs. Connection is made per designated pins for each output. Also available on +3.3Vdc_Aux (see ordering info)
Protocol	Per VITA 46.11 System Management Bus
Status LED	See LED Status table below

LED Status

LED State	Meaning
Off	Input Low
Green (Steady)	Vout OK; All outputs are good
Red (Steady)	Fail; Follows same logic as FAIL* signal
Blinking Green	Unit disabled
Blinking Red	Over Voltage or Over Temperature (all outputs are off)

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Power Status

Control Input States		Power Output States	
ENABLE*	INHIBIT*	+3.3V_AUX	VS1/VS2, VS3, +12V_Aux & -12V_Aux
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

I²C Communication

1. Hardware Interface.

Electrical interface is based on I2C parameters at 100 kHz. The backplane or I2C master controller should provide pull up resistors on SDA and SCL lines to a 3.3V rail.

2. Address.

The I2C Hardware Address (per VITA 46.11 Rev 0.15) is 7 bits. The default base address is 0x20. *GA0 through *GA4 provide the 5 LSB's for the address.

The *GA pins have 3.32K pull-up resistors to a 3.3V rail. The resistors and the 3.3V rail are internal to the power supply. When left open, the address will be 0x20, otherwise, the address will be as described in the table below.

Signal						I2C Address
*GAP	*GA4	*GA3	*GA2	*GA1	*GA0	
Pin A5	Pin B5	Pin A4	Pin B4	Pin C4	Pin D4	
Gnd	High	High	High	High	High	0x20
High	High	High	High	High	Gnd	0x21
High	High	High	High	Gnd	High	0x22
Gnd	High	High	High	Gnd	Gnd	0x23
High	High	High	Gnd	High	High	0x24
Gnd	High	High	Gnd	High	Gnd	0x25
Gnd	High	High	Gnd	Gnd	High	0x26
High	High	High	Gnd	Gnd	Gnd	0x27

If the unit detects an error on the *GAP input setting, it will respond to address 0x20.

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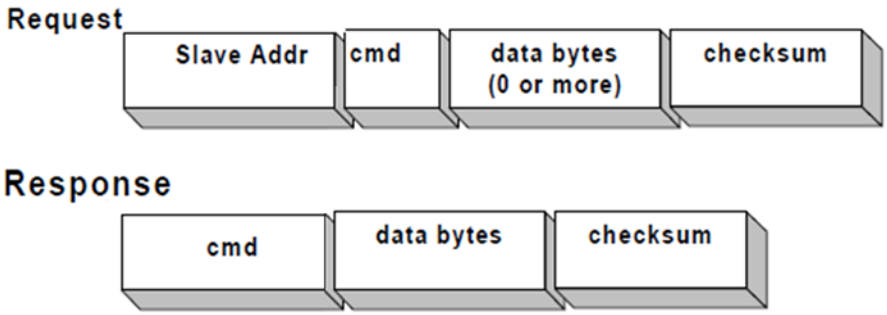
3. Data Read - Get Sensor Reading results



	Byte	Data Field	Data
Request Data	1	cmd	See table
	2 to n-1	Data If Required by cmd or Zero ChkSum* if no Data required.	
	n	Zero ChkSum* if Data was required by cmd	
Response Data	1	Completion Code – Echo cmd Number	
	2 to n-1	Per cmd Response	
	n	Zero ChkSum	

*Note : Slave address should not be included in Zero Checksum calculation.

4. Commands

Sensor #	Name	Description
21H	Composite Sensor	64 bytes of scanned sensor data. Data is continually scanned and available for report. Data consists of 2 bytes of data for each of the 11 sensors and FRU data.
55H	Status Write Command	Writes Status byte on Composite Sensor.
44H	Firmware release date	22 byte response. Month/Day/Year Hr/Min/Sec in ASCII form.

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4.1 Composite Sensor Read Command – 21H

Response BYTE #	Data Type	Meaning
0	Completion Code – 21h	Echo of the command
1	Status Register 0, MS Bit First	Refer to table below
2-3	Signed Integer, MSB First	Temperature as follows °C = (Reading * 100 / 16384)
4-5	U Integer, MSB First	Voltage on VS1, 12V = 16384
6-7		Reserved
8-9	U Integer, MSB First	Voltage on VS3, 5V = 16384
10-11	U Integer, MSB First	Voltage on 3.3Aux, 3.3V = 16384
12-13	U Integer, MSB First	Voltage on +12V Aux, 12V = 16384
14-15	U Integer, MSB First	Absolute Voltage on -12V Aux, 12V = 16384
16-17	U Integer, MSB First	Current on VS1, 30A = 16384
18-19		Reserved
20-21	U Integer, MSB First	Current on VS3, 50A = 16384
22-23	U Integer, MSB First	Current on 3.3Aux, 20A = 16384
24-25	U Integer, MSB First	Current on +12VAux, 3A = 16384
26-27	U Integer, MSB First	Absolute Current on -12VAux, 3A = 16384
28-29	U Integer, MSB First	Internal Reference, 2.5V = 16384
30-31		Reserved
32-51	Character String	Part Number
52-53	U Integer, MSB First	S/N Hi
54-55	U Integer, MSB First	S/N Low
56-57	U Integer, MSB First	Date Code (Year/Week)
58-59	U Integer, MSB First	Hardware Rev
60-61	U Integer, MSB First	Firmware Rev.
62	Reserved	Reserved
63	Zero Checksum	Value required to make the sum of bytes 0 to 62 add to a multiple of 256 (decimal).

Status Reg 0		R/Set	R/Set	R/W	R/W	R/W	R	R
Bit	7	6	5	4	3	2	1	0
	x	FAIL	OTWarning	SWPriority	*SW Inh	*SW En	*HW Inh	*HW En

Bits 5 AND 6 (OTWarning - FAIL) are Read and write. They are clear at startup. User can set them with a Status Write command. Hardware will clear them if there is a fault.

Bit 4 (SWPriority) is Read and write. It is clear at Startup. When clear the unit will be controlled by the hardware enable and inhibit signals. When set, the unit will be controlled by the SW inhibit and enable signals.

Bits 3 and 2 (SWInh SWEn) are read and write. Their logic works the same as the logic for the hardware Enable and Inhibit.

*SWEnable	*SWInhibit	OUTPUTS
0	0	INHIBIT (3.3V Aux is On, all other outputs are off)
0	1	ON
1	0	OFF
1	1	OFF

Bits 1 and 0 (HWIn - HWEn) are read only. They show the state of *Enable and *Inhibit pins while SWPriority is low.

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4.2 Status Write Command - 55H

BYTE #	Data Type	Meaning
0	U Character – 55H	Command
1	U Character	Data
2	Zero Checksum	Value required to make the sum of bytes 0 and 1 add to a multiple of 256 (decimal).

The command to write to Status byte is 55h, followed by 8-bit data then zero checksum.

Example: To send a command to clear the faults and turn on all the outputs, the following sequence must be sent.
55h 78h 33h;
55h is the command needed to write to status byte zero.
78h data for byte zero,
Bit 7 set: don't care bit.
Bit 6 set: FAIL signal is high, software will clear it if unit fails
Bit 5 set: OTWarning signal is high, software will clear it if unit is close to 75 degrees.
Bit 4 set: Software has priority to enable/disable unit.
bit 3 set: SWInhibit is high
bit 2 low: SWEnable is low.
33h Value to achieve a sum of zero.

4.3 Firmware release date – 44H

Response BYTE #	Data Type	Meaning
0	Completion Code – 44H	Echo of the command
1-20	Character String	Date
21	Zero Checksum	Value required to make the sum of bytes 0 to 20 add to a multiple of 256 (decimal).

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Input Pinout Designations (P0)

Pin #	Rated Current (A)	Name	Description
P7	40	ACL/L1 (+270 VDC)	AC Phase 1 or +270 VDC input
P6	40	L2	AC Phase 2
P5	40	L3	AC Phase 3 or +270 VDC Return
P4	40	ACN	AC Neutral
P3	40	POS_FILT_OUT	Not Used
P2	40	NEG_FILT_OUT	Not Used
P1	40	CHASSIS	Chassis Ground

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Output Pinout Designations (P1)

Pin #	Rated Current (A)	Pin Name (Std VITA 62)	Description		Pin #	Rated Current (A)	Pin Name (Std VITA 62)	Description
P10	40	VS1/VS2 *NOTE 1	VS1/VS2 combined into one output		**D5**	<1A	SM1	System Management Bus (I^2C Data)
P9	40	VS1/VS2 *NOTE 1	VS1/VS2 combined into one output		**A4**	<1A	GA3*	Geog. Address
A9	<1A	VS1/VS2_SENSE	Remote Sense for VS1/VS2		**B4**	<1A	GA2*	Geog. Address
B9	<1A	RESERVED			**C4**	<1A	GA1*	Geog. Address
C9	<1A	VS3_SENSE	Remote Sense for VS3		**D4**	<1A	GA0*	Geog. Address
D9	<1A	UD0	User Defined		**A3**	<1A	UD2/+12Vdc_Aux	Used for +12 VDC_Aux
A8	<1A	VS1_SENSE_RTN	Remote Sense Return		**B3**	<1A	+12V_AUX ***NOTE 3	+12 VDC_Aux Output
B8	<1A	RESERVED			**C3**	<1A	RESERVED	
C8	<1A	VS3_SENSE_RTN	Remote Sense Return for VS3		**D3**	<1A	RESERVED	
D8	<1A	UD1	User Defined		**P6**	40	VS3**NOTE 2	VS3 Output
A7	<1A	VS1/VS2_SHARE	Current Share for VS1/VS2		**P5**	40	VS3**NOTE 2	VS3 Output
B7	<1A	*+3.3_Aux Share*	*Optional*		**P4**	40	POWER_RETURN	Common Output Return
C7	<1A	VS3_SHARE	Current Share for VS3		**P3**	40	POWER_RETURN	Common Output Return
D7	<1A	SIGNAL_RETURN	Common Signal Return		**A2**	<1A	VBAT *(optional)*	Connected Internally to +3.3 VDC_Aux
P8	40	POWER_RETURN	Common Output Return		**B2**	<1A	FAIL*	Active Low Open-Drain
P7	40	POWER_RETURN	Common Output Return		**C2**	<1A	INHIBIT*	Used with ENABLE* (see Power Status Table, page 5)
A6	<1A	SM2	System Management Bus		**D2**	<1A	ENABLE*	Used with INHIBIT* (see Power Status Table, page 5)
B6	<1A	SM3	System Management Bus		**A1**	<1A	UD3 or SMB_Alert	User Defined / SMB_Alert (option)
C6	<1A	-12V_AUX ***NOTE 3	-12 VDC_Aux Output		**B1**	<1A	UD4/-12Vdc_Aux	Used for -12 VDC_Aux
D6	<1A	SYSRESET*	System Reset (Active low open-collector)		**C1**	<1A	UD5 /+3.3_Aux Sense	User Defined / +3.3_Aux Sense
A5	<1A	GAP*	Geographical Address (Parity)		**D1**	<1A	UD6 / +3.3_Aux Sense Rtn	User Defined / +3.3_Aux Sense Rtn
B5	<1A	GA4*	Geographical Address		**P2**	40	3.3V_AUX	+3.3 VDC_Aux Output
C5	<1A	SM0	System Management Bus (I^2C Clock)		**P1**	40	POWER_RETURN	Common Output Return

***NOTE 1: On Standard VITA 62 output configuration, VS1 and VS2 pins are combined into one output**

***NOTE 2: On Heavy +12vdc output configuration, VS1, VS2 and VS3 pins are combined into one output (+5Vdc output is not available)**

***NOTE 3: On Heavy +12vdc output configuration, +/-12Vdc_Aux outputs are not available)**

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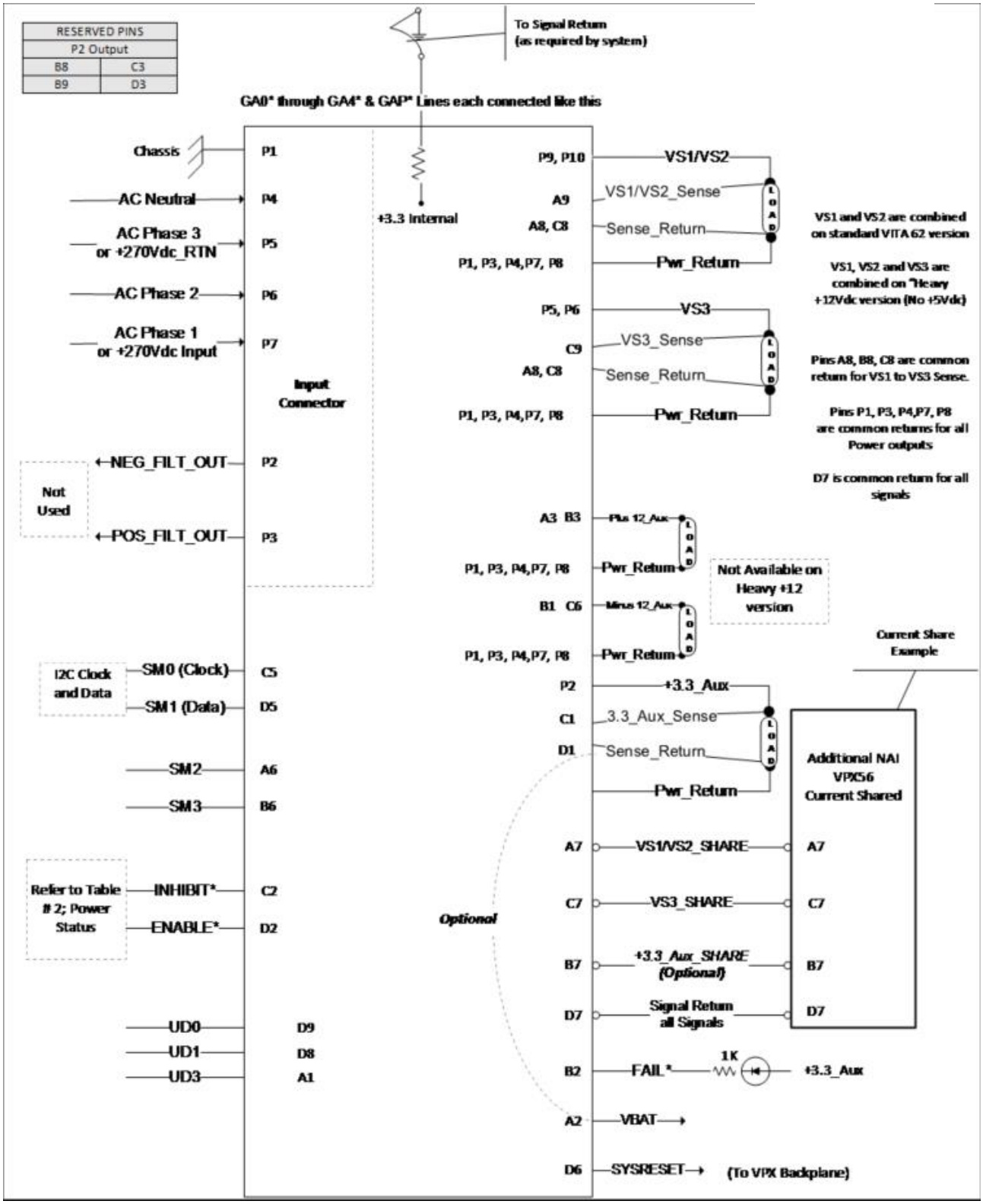
VPX56H2-6 Connections



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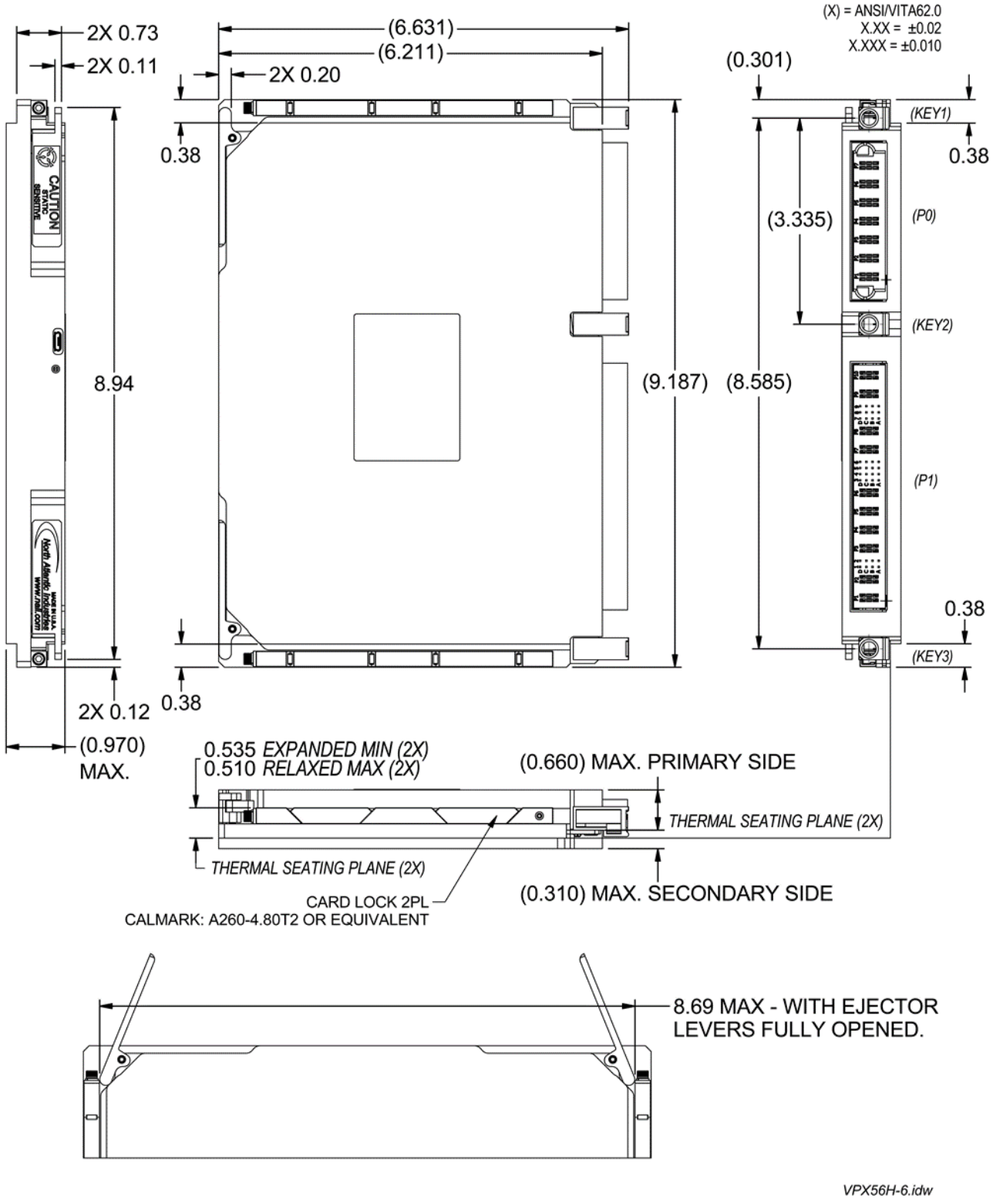
Mechanical Layout



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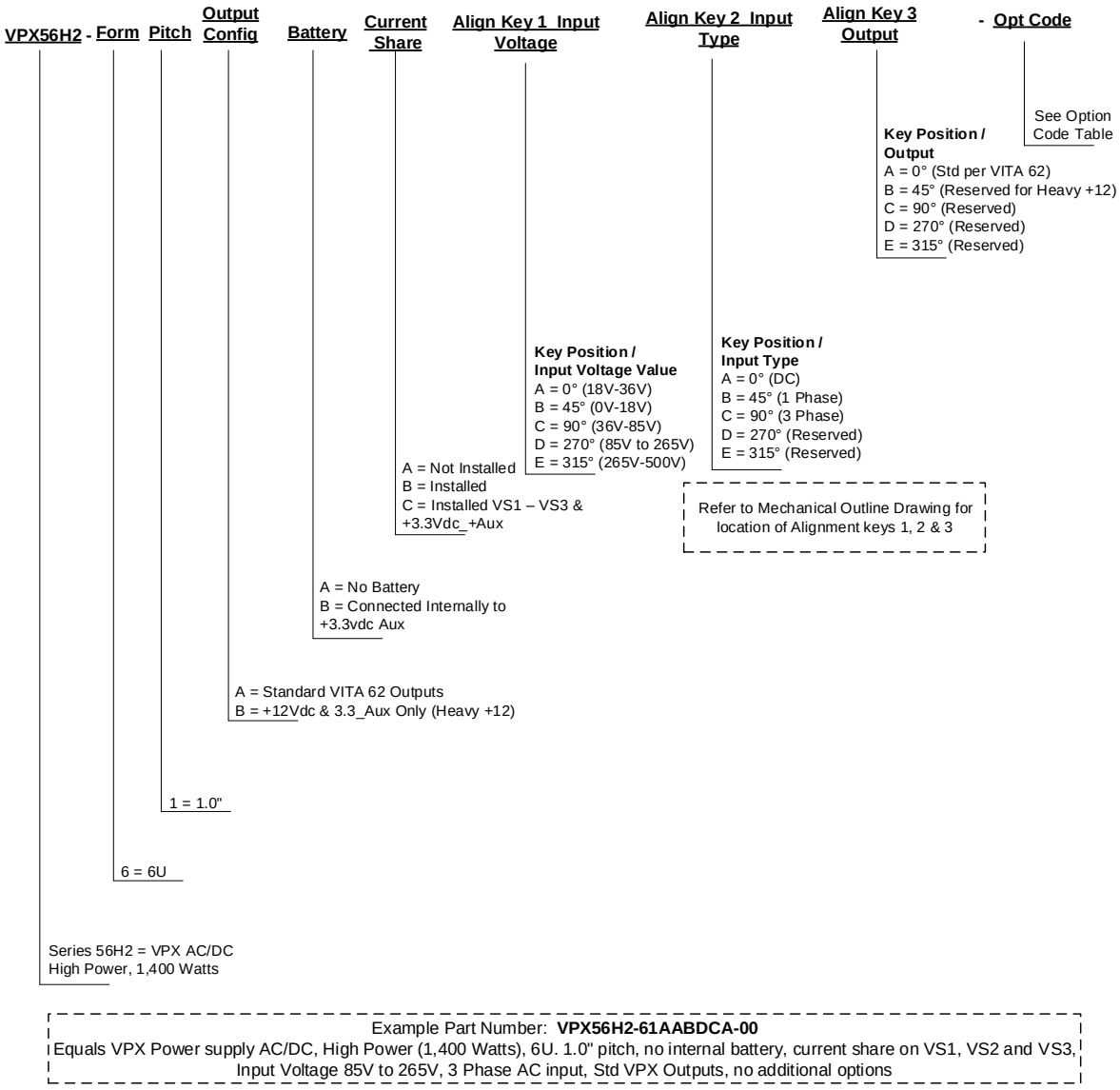
Ordering Information



Option Code Table

Code	Description	Output Configuration
00	Standard Unit, no additional options	VS1/VS2 = +12 VDC @ 80 A Total VS3 = +5 VDC @ 50 A +3.3 VDC_Aux = +3.3 VDC @ 20 A ±12 VDC_Aux @ 3 Amps each

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