Function Module DSx

Model: DSx
Description: Synchro/Resolver Simulation

Module Options

Module ID		No. of Channels	Full Scale Output Voltage (RMS VL-L)	Output Load	Frequency Range (Hz)
Synchro	Resolver				
DS1	DR1	1	2-28	3 VA @ 28 V_{RMS}	47-1k
DS2	DR2	1	2-28	3 VA @ 28 V_{RMS}	1k-5k
DS3	DR3	1	2-28	3 VA @ 28 V_{RMS}	5k-10k
DS4	DR4	1	2-28	3 VA @ 28 V_{RMS}	10k-20k
DS5	DR5	1	28-90	3 VA @ 90 V_{RMS}	47-1k
DSA	DRA	2	2-28	2.2 VA @ 28 V_{RMS}	47-1k
DSB	DRB	2	2-28	2.2 VA @ 28 V_{RMS}	1k-5k
DSC	DRC	2	2-28	2.2 VA @ 28 V_{RMS}	5k-10k
DSD	DRD	2	2-28	2.2 VA @ 28 V_{RMS}	10k-20k
DSE	DRE	2	28-90	2.2 VA @ 90 V_{RMS}	47-1k
DSJ	DRJ	3	2-28	0.5 VA @ 28 V_{RMS}	47-1k
DSK	DRK	3	2-28	0.5 VA @ 28 V_{RMS}	1k-5k
DSL	DRL	3	2-28	0.5 VA @ 28 V_{RMS}	5k-10k
DSM	DRM	3	2-28	0.5 VA @ 28 V_{RMS}	10k-20k
DSN	DRN	3	28-90	0.5 VA @ 90 V_{RMS}	47-1k

There are three types of D/S and D/R modules:

- 3-Channel Modules: These high-density modules have a lower power output drive (0.5 VA per channel, maximum). The lower power output drive is ideal for driving solid-state input instruments, gauges, and Synchro Booster Amplifiers (SBAs).
- 2-Channel Modules: The 2-channel modules have a standard power output of 2.2 VA per channel, maximum.
- Single-Channel Modules: The single-channel modules have a high-power output drive capability (3 VA per channel, maximum).

Programmable Features:

- Signal Loss Threshold
- Reference Loss Threshold
- Rotation Mode
- 2-Speed Simulation

Measured signals:

- Individual channel input Reference and Signal voltages
- Individual channel input Reference Frequency
- Individual channel Current

Built-In Test (BIT) / Diagnostic Capability

Two different tests (one on-line and one off-line) can be selected.

The Online (D2) Test initiates automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output angle to the commanded angle. Each channel is individually checked to an accuracy of 0.2° and each D/S Signal output is continually monitored. User can periodically clear to 00h and then read Test (D2) Verification register again, after 0.1 seconds, to verify that background bit testing is activated. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled.

The (D3) Test initiates a BIT test that generates and tests 24 different angles to a test accuracy of 0.2 °. Results can be read from registers.

Embedded Soft Panel (ESP) allows easy access to each channels information availble for Download

For more information contact ティー・ピー・ティー株式会社 (TPT K.K.)

Telephone: 81-3-5832-7350
TPT KK: Contact
http://www.tptech.co.jp

5/6/21 Rev. A