

30 VA Synchro Booster Amplifier

30 VA Synchro Booster Amplifier

For Commercial or Military Applications



44PA1-4B1 Type Configuration

FEATURES

- 30 VA / 90 VL-L Synchro Output
- Resolver 5.0VL-L; 6.81VL-L direct coupled, or 90VL-L, transformer isolated input options
- ± 0.05 deg. Accuracy / Infinite Resolution
- 60 Hz or 400 Hz option
- Remote ON/OFF option
- Built-In-Test / Output Fault Monitor
- Wrap output capability for direct signal monitoring
- No calibration requirements
- Rugged construction
- Input and output protection



44PA1-4A0 Type Configuration

DESCRIPTION:

This Military-grade stand-alone unit is the perfect solution when higher output power or 60 Hz drive capability is required. The amplifier accepts either a High voltage Synchro input or a low voltage Resolver input and delivers 30 VA of Synchro power that will drive most of the existing 60 Hz or 400 Hz Control Transformers or Torque Receivers.

The amplifier can be remotely turned "ON" or "OFF" and is therefore usable for redundant applications. All signal inputs are transformer isolated and logic inputs and outputs are opto-isolated. Since power is derived from the reference rather than DC supplies, heat dissipation is reduced by 50%.

Built-In-Test (BIT) capability is included to monitor over-temperature and over-current conditions. Wrap around testing (isolated, low level signal output) will seamlessly interface with the self-test capability of North Atlantic Industries broad range of intelligent multifunction/synchro cards.

This amplifier requires no adjustments or calibration, has ruggedized construction and is electrically protected as well. It is protected from output short circuits, current overloads, load voltage transients, reference transients, and over-temperature.

Two (2) enclosures are offered, both containing all the electrical improvements described above;

The "**A**" enclosure is a standard, replacement enclosure (matching footprint of DDC SBA series). Does not include "wrap" output functionality.

The "**B**" enclosure is a mechanically improved version with built-in captive screws and also allows for wraparound test (example: inter-connection with any of NAI's intelligent multifunction/synchro cards to provide complete, accurate, dynamic self test). This enclosure also offers Remote ON/OFF capability.

TABLE OF CONTENTS

FEATURES	1
DESCRIPTION:.....	1
SPECIFICATIONS:	3
RESOLUTION:.....	3
ACCURACY:	3
INPUT FORMAT:	3
INPUT IMPEDANCE:.....	3
OUTPUT FORMAT:	3
LOAD:	3
PROTECTION:	3
ON/OFF: (DIS)	3
BIT:.....	3
WRAP-AROUND TEST:.....	3
GAIN TOLERANCE:.....	3
MTBF:	3
POWER:.....	3
REFERENCE OUTPUT:.....	3
TEMP. OPERATING:	3
TEMP. STORAGE:	3
HEAT TRANSFER:.....	3
WEIGHT:	3
SIZE:.....	3
ENCLOSURE:	3
CONNECTOR PIN-OUT:.....	4
"B" ENCLOSURE	4
"A" ENCLOSURE	4
BIT AND POWER ON/OFF CONNECTION DIAGRAMS:	5
44PA1 TO NAI'S 64DS1 OR 64CS3 INTERCONNECTION (EXAMPLE);	6
MECHANICAL:	7
PART NUMBER:.....	8
REVISION PAGE:.....	9

SPECIFICATIONS:

Resolution:	Infinite
Accuracy:	$\pm 0.05^\circ$ for Passive loads (CT, etc); $\pm 0.167^\circ$ for TR loads
Input format:	Resolver 5.0VL-L; 6.81VL-L direct coupled, or 90VL-L, transformer isolated. (See P/N)
Input Impedance:	190 K Ω min for 90VL-L input; 14 K Ω min for Resolver inputs.
Output format:	Synchro, 90V _{L-L} , Short circuit proof. Synchro outputs are floating, therefore, one leg may be grounded.
Load:	Passive loads: 202 Ω ; Torque receivers: 6 Ω
Protection:	Output is short circuit protected. However, sufficient power is provided to switch a TR through a 180 ° angle. Recovery from a short circuit is within 4 seconds. TR's are monitored for false null and should a TR latch at a false null, an optional kick circuit can be wire programmed to force the TR to start moving toward the correct angle.
ON/OFF: (DIS)	Output can be remotely turned ON or OFF, opto-isolated. TTL compatible. ON is "0" at 2 mA; OFF is "1" at 0 mA.
BIT:	Built-In-Test (BIT) is an overload indicator (signal output, opto-isolated TTL compatible). Normal is "0", Fault is "1". Logic "1" indicates that output is turned OFF caused by over-temperature. For an over-current condition, the BIT signal will also be energized but the outputs will not be turned off. There is a time delay on over-current sensing to allow for a temporary over-current condition when driving a TR. BIT, used in conjunction with the Wrap-around test signals, provides comprehensive unit BIT capability.
Wrap-around test:	Applies only to "B" enclosure configurations. The Synchro output, using a separate isolation transformer, is converted to 2V _{L-L} Resolver signal (WA Sin, WA Cos and WA return) which can be fed into one of our Intelligent S/D - D/S Cards where it is seamlessly incorporated into the card's background BIT testing that verifies accuracy or signal loss. Legacy 44PA1 models provide the wrap signals 180 degrees out of phase as compared with the output drive signals. Because of the different accepted resolver wiring conventions, the 44PA1 can now be configured to have the wrap signals either in-phase or 180 degrees out of phase with the drive signals (see part number).
Gain Tolerance:	$\pm 2\%$
MTBF:	45,000 hours min.
Power:	115 Vrms 60 or 400 Hz (See Part Number).
Reference output:	If needed, a 2.0 Vrms output is provided. Developed from power input. (B enclosures only, See P/N)
Temp. operating:	-40°C to +71°C. Base temperature not to exceed +71°C
Temp. storage:	-55°C to +85°C.
Heat transfer:	Heat to be dissipated is 1.5 watts max. per VA delivered
Weight:	4 lb. max.
Size:	7.40 x 5.09 x 2.48
Enclosure:	DDC SBA-series footprint compatible ("A enclosure.) A "B" enclosure is available with integrated mounting & other features. (See "Mechanical") All units are enclosed. Finish is alodine per MIL-C-5541, class 3

CONNECTOR PIN-OUT:

For **resolver** input; S1 with respect to S3 is + sine (S1 = + sin, S3 = - sin)
S4 with respect to S2 is + cosine (S4 = + cos, S2 = - cos)

- Notes: 1. This is a "legacy" naming convention definition and SIN/COS (+) and (-) are "reversed" in comparison to the modern-day NAI resolver naming convention.
2. Unit may be operated with AC Ref Hi and Ref Lo "swapped"; SIN/COS (+) and (-) naming convention definitions will reverse and be in-line with the modern-day NAI resolver naming convention definitions.

"B" Enclosure

Front panel Connector (J1): DC37P; Mate: DC37S (Connector on enclosure "short" side)

Pin		Pin		Pin		Pin		Pin		Pin	
1	S1 out	5	WA Cos	7	Ref Lo In 115V	10	S3 in (90 VL-L)	17	See note	19	ON/OFF Input Hi
2	S3 out	23	WA return	8	Ref Hi out 2.0V	28	S2 in (90 VL-L)	34	See note	36	ON/OFF Input Lo
20	S2 out	37	Chassis	27	Ref Lo out 2.0V	13	S3 in (5.0 VL-L)	18	BIT Output Hi	6	K
4	WA Sin	26	Ref Hi In 115V	9	S1 in (90 VL-L)	31	S2 in (5.0 VL-L)	35	BIT Output Lo	24	CO

Notes: For the "B" enclosure:

- The input can be either Synchro (90 V_{L-L}) or Resolver (5.0 V_{L-L} or 6.81 V_{L-L}). See P/N.
- For resolver input (options 2 and 4), connect Resolver inputs (-sine) and (-cosine) to WA return.
- To Enable kick circuit for Torque Receivers; connect "K" (pin 6) to "CO" (pin 24). See P/N.
- Pins 13 and 31 are for 5.0 V_{L-L} or 6.8 V_{L-L} signal inputs (See P/N).
- Remote ON/OFF, using a differential driver, is accomplished by connecting to pins J1-19 (HI) and J1-36 (LO).
- Remote ON/OFF, using a single-ended driver, is accomplished by connecting pin J1-19 to a customer supplied + 5 V_{DC} and switching pin J1-36 to logic "0" (ground) to turn "ON", logic "1" (+ 5 V_{DC}) or "open" to turn "OFF". ON at 2 mA; OFF at 0 mA.
- To turn amplifier ON permanently, connect pin J1-17 to pin J1-34
- BIT output, using a single-ended driver, is accomplished by connecting pin J1-18 to a customer supplied +5 V_{DC} (current limited with a user supplied 4.99K ohm resistor) and pin J1-35 to ground. A Fault will set pin 18 to +5 V_{DC} (logic "1") and normal operation will be at almost 0 V (logic "0").

"A" Enclosure

Front panel Connector (J2): DB25P; Mate: DB25S (Connector on enclosure "long" side)

Pin		Pin		Pin		Pin		Pin	
1	+5V	6	K	11	S4 In	16	Ground	21	S2 Out
2	BIT Output	9	S1 In	12	S2 In	17	S3 Out	23	R Hi In 115V
4	S1 Out	10	S3 In	14	ENABLE	18	CO	24	R Lo In 115V

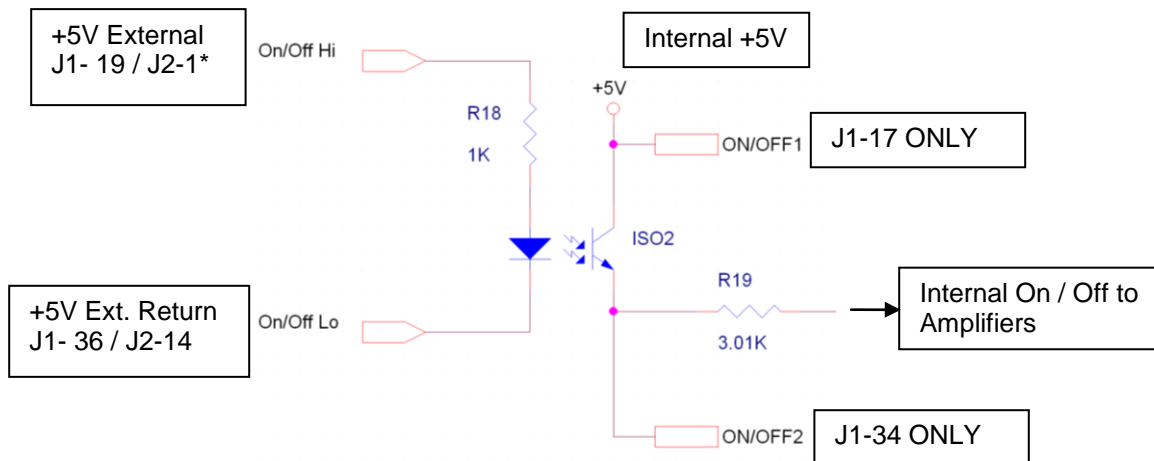
Notes: For the "A" enclosure:

- Input can be either Synchro (90 V_{L-L}) or Resolver (5.0 V_{L-L} or 6.81 V_{L-L}) (see P/N).
- To Enable kick circuit for Torque Receivers, connect "K" (pin J2-6) to "CO" (pin J2-18) (see P/N).
- Bit output, requires a customer supplied +5 V_{DC} high to pin 1 and 0 V_{DC} low (logic -ground) to pin J2-16. A Fault will set (pin J2-2) to +5 V_{DC} (logic "1") and normal operation will be at almost 0_{DC} V (logic "0").
- "A0" unit outputs are turned on with (pin J2-1) connected to a customer supplied (+5 V_{DC}) and "ENABLE" (pin J2-14) switched to TTL logic "0" (ground). Outputs are off with (pin J2-14) open or connected to TTL logic "1" (+5 V_{DC}).
- "A1" unit outputs are always "ON" (no +5V_{DC} high/low required for output enable).

The 44PA1 series is capable of meeting the conditions and requirements of MIL-STD-202 (see table below).

MIL-STD-202 TEST METHODS		
METHOD	CONDITION	COMMENT
204	C	10 G, 2KHz Vibration
213	A	50 G, 11 ms Shock
106*	---	Moisture
107	A	Thermal Shock
101*	B	Salt Spray
105	B	50 K feet altitude
NOTES: * When PC board has been conformal coated (see part number)		

BIT and POWER ON/OFF CONNECTION DIAGRAMS:



NOTES:

- J2 Connections are for "A" enclosures. J1 Connections are for "B" enclosures.
- For Amplifier "Always On", "A" Enclosures, Ext. +5V to J2-1 & +5V Ret. to J2-14.
- For Amplifier "Always On", "B" Enclosures, Jumper J1-17 to J1-34 or, Ext. +5V to J1-19 & +5V Ret. to J1-36.
- * - J2-1 (+5V Ext.) is internally connected to "On/Off Hi"

Fig. 1
44PA1 Amplifier On / Off Circuit

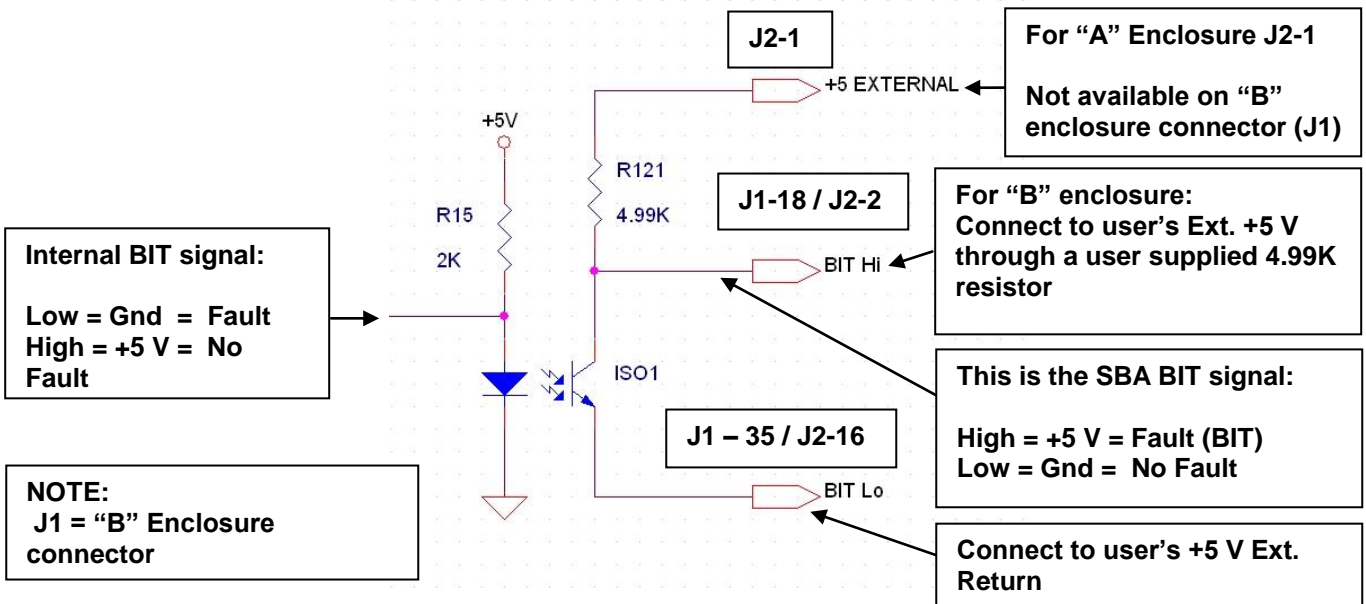


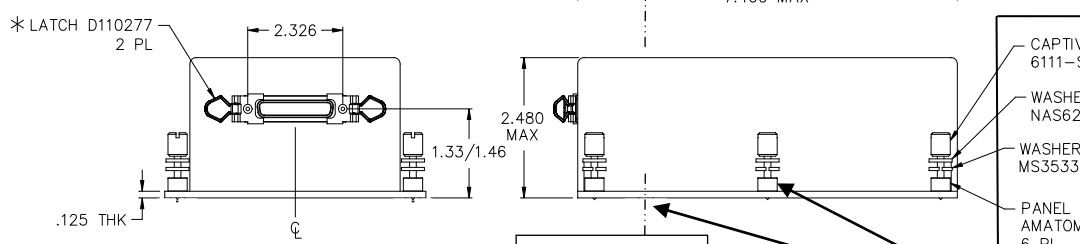
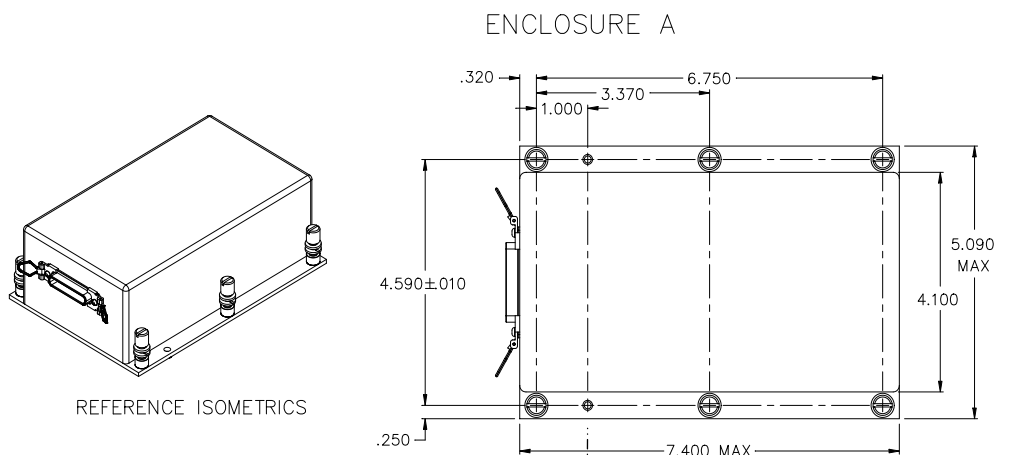
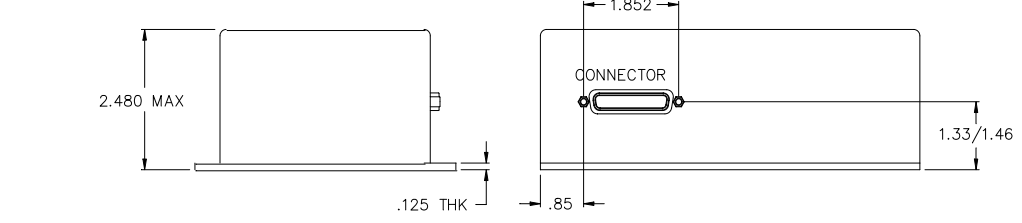
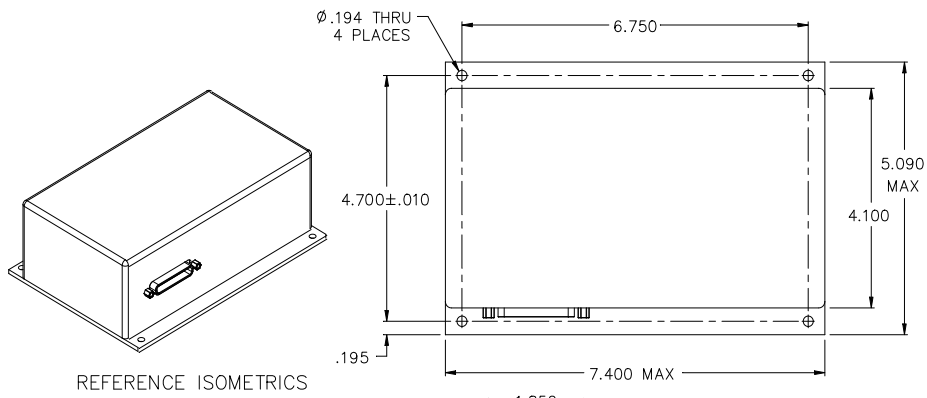
Fig. 2
44PA1 Built-In-Test (BIT) Circuit

44PA1 TO NAI'S 64DS1 OR 64CS3 INTERCONNECTION (EXAMPLE): (Channel 1 as Example)

44PA1				64DS1				64CS3			
"B" Enclosure		"A" Enclosure		J1 & J2		P2 Only		J1		P2 & P0	
Pin		Pin		Pin	J1	Pin	P2	Pin	J1	Pin	P2
13	S3 in (5 / 6.8 V _{LL} RSL)	10	S3 In	J1.19	S3 Ch.1	P2.22c	S3 Ch.1	J1.36	S3 Ch.1	P2.14a	S3 Ch.1
31	S2 in (5 / 6.8 V _{LL} RSL)	12	S2 In	J1.36	S2 Ch.1	P2.20c	S2 Ch.1	J1.19	S2 Ch.1	P2.12a	S2 Ch.1
23	WA return	9	S1 In	J1.37	S1 Ch.1	P2.18c	S1 Ch.1	J1.37	S1 Ch.1	P2.10a	S1 Ch.1
23	WA return	11	S4 In	J1.18	S4 Ch.1	P2.24c	S4 Ch.1	J1.18	S4 Ch.1	P2.16a	S4 Ch.1
4	WA Sin	--		J2.1	Sine Hi Ch.1	P2.3d	Sine Hi Ch.1	J1.7	Sine Hi Ch.1	P2.5z	Sine Hi Ch.1
5	WA Cos	--		J2.20	Cos Hi Ch.1	P2.5d	Cos Hi Ch.1	J1.25	Cos Hi Ch.1	P2.3z	Cos Hi Ch.1
23	WA return	--		J2.2	Common Ch.1	P2.4d	Common Ch.1	J1.6	Common	P2.7z	Common Ch.1
8	Ref Hi out 2V	--		J1.35	RHi in 2V	P2.29c	RHi in 2V Ch.1	J1.35	RHi in	P2.28a	RHi in 2V Ch.1
27	Ref Lo out 2V	--		J1.17	Rlo in 2V Ch.1	P2.27c	Rlo in 2V Ch.1	J1.17	Rlo in 2V Ch.1	P2.27a	Rlo in 2V Ch.1
18	BIT Hi Output	2	BIT Output			P2.1a	BIT Hi Ch.1			P0.12e	BIT Hi Ch.1
35	BIT Lo Output	--				P2.2a	BIT Lo Ch.1			P0.12d	BIT Lo Ch.1
19	ON/OFF In Hi	--				P2.1z	On/Off Hi			P0.6e	On/Off Hi Ch.1
36	ON/OFF In Lo	--				P2.3z	On/Off Lo Ch.1			P0.6d	On/Off Lo Ch.1
1	S1 out	4	S1 Out		N/A		N/A		N/A		N/A
2	S3 out	17	S3 Out		N/A		N/A		N/A		N/A
20	S2 out	21	S2 Out		N/A		N/A		N/A		N/A
26	Ref Hi in 115V	23	R Hi in		N/A		N/A		N/A		N/A
7	Ref Lo in 115V	24	R Lo in		N/A		N/A		N/A		N/A
9	S1 in (90 VL-L)	--			N/A		N/A		N/A		N/A
10	S3 in (90 VL-L)	--			N/A		N/A		N/A		N/A
28	S2 in (90 VL-L)	--			N/A		N/A		N/A		N/A
37	Chassis	--			N/A		N/A		N/A		N/A
17	See note 2				N/A		N/A		N/A		N/A
34	See note 2				N/A		N/A		N/A		N/A
6	K	6	K		N/A		N/A		N/A		N/A
24	CO	18	CO		N/A		N/A		N/A		N/A
		1	+5V		N/A		N/A		N/A		N/A
		14	ENABLE		N/A		N/A		N/A		N/A
		16	Ground		N/A		N/A		N/A		N/A

Notes: 1. 64DS1 & 64CS3 front panel J connectors and rear P connectors are in parallel. P2 is always active
 2. To turn amplifier ON permanently, connect pin 17 to pin 34.

MECHANICAL:



- (B2) & (B3)
Metric captive hardware enclosure options
- METRIC CAPTIVE PANEL SCREW
M5 THREAD
- METRIC PANEL SCREW RETAINER
M5 THREAD
- CAPTIVE PANEL SCREW
6111-SS-1032-7, 6 PL
- WASHER, FLAT
NAS620C-10, 6 PL
- WASHER, LOCK
MS35338-138, 6 PL
- PANEL SCREW RETAINER
AMATOM 6254-SS-1032-7
6 PL
- (B0) & (B1)
Captive hardware for enclosure options

* INSTEAD OF THE LATCHES, FEMALE LOCK POSTS CAN BE SUPPLIED. THIS ENABLES USERS TO LOCK THE MATING CONNECTOR TO THE ENCLOSURE BY USING SCREWS.

- (B4) & (B5) enclosure option(s):
Captive panel screw(s) / hardware and inserts REMOVED from unit baseplate.
- NO baseplate securing hardware provided. Baseplate thru-holes only:
- 1) 0.270" dia. thru-hole, 6 pls. (in lieu of captive screw/hardware)
 - 2) 0.187" dia. thru-hole, 2 pls.

Part Number Designation:

44PA1- X X XX X - XX - XX

INPUT FORMAT

- 1 = 90 V_{L-L} Synchro input
- 2 = 5 V_{L-L} Resolver input
- 4 = 6.81 V_{L-L} Resolver input

REF. TRANSFORMER / KICK CIRCUIT OPTIONS

For "A" Mechanical Enclosure ONLY:

- 0 = No reference output transformer / Kick Circuit externally enabled
("K" to "CO" internal jumper removed)

For "B" Mechanical Enclosure ONLY:

- 0 = No reference output transformer / Kick Circuit internally enabled
("K" to "CO" Internal jumper installed)
- 1 = No reference output transformer / Kick Circuit externally enabled
("K" to "CO" internal jumper removed)
- 2 = Reference output transformer / Kick Circuit externally enabled
- 3 = Reference output transformer / Kick Circuit internally enabled

MECHANICAL

- A0 = Standard "A" enclosure (with connector female lockposts)
(outputs default "OFF" – use ENABLE pin 14 to turn outputs "ON" requires +5V_{DC})
- A1 = Standard "A" enclosure (with connector female lockposts)
(outputs always "ON" - does not require +5V_{DC})
- B0 = "B" enclosure with SAE captive chassis screws; (with connector latches)
- B1 = "B" enclosure with SAE captive chassis screws; (with connector female lock posts)
- B2 = Same as B0 with metric captive chassis screws
- B3 = Same as B1 with metric captive chassis screws
- B4 = "B" enclosure with connector latches and NO baseplate hardware
- B5 = "B" enclosure with connector female lock posts and NO baseplate hardware

PCB CONFORMAL COATING *1

- 0 = No PCB conformal coat
- K = PCB conformal coat

OPERATING FREQUENCY / WRAP OUTPUT PHASING

(note: Wrap function only applies to "B" enclosures)

- 60 = 60 Hz (for "A" enclosure only) / Wrap not available
- 60 = 60 Hz (for "B" enclosure) / Legacy wrap 180 deg out of phase with output drive signal
- 61 = 60 Hz (for "B" enclosure) / Wrap in phase with output drive signal
- 62 = 60 Hz (for "B" enclosure) / No Wrap
- 40 = 400 Hz (for "A" enclosure only) Wrap not available
- 40 = 400 Hz (for "B" enclosure) / Legacy wrap 180 deg out of phase with output drive signal
- 41 = 400 Hz (for "B" enclosure) / Wrap in phase with output drive signal
- 42 = 400 Hz (for "B" enclosure) / No Wrap

SPECIAL OPTION CODE (or leave blank for none)

(Special Options – contact factory)

Part Number Notes:

- *1: For legacy part numbering; if no part number designator (blank) for PCB conformal coating option, then PCB has no conformal coat.

REVISION PAGE:

Revision	Description of Change	Engineer	Date
P1	Initial Release	GS	04/30/02
P2	Edits A & B enclosure description	GS	05/31/02
P3	Page 2, description of the "A" type and part number to include the "A1" in the part number, to use the unit without a +5V power supply.	GS/JP	06/18/02
P3.1	Changes to the NOTES section for the "A" enclosure, explaining in greater detail how the unit works AND clarifying the part number.	GS/JP/AF	07/08/02
P3.2	Enclosure height from 2.62 to 2.48. Changed connector location height	FH	12/22/02
P3.3	For resolver input, either enclosure; $S3 = -\sin$ $S1 = +\sin$ $S2 = -\cos$ $S4 = +\cos$ For resolver input (options 2 and 4), Encl. "A" connect resolver inputs S1 & S4 to WA return. Ref and S2 & S3 are 2 V rms signals. Adds 44PA1 to 64Ds1 channel connection table.	GS	12/08/03
P3.4	Add "2" for 5 VL-L Resolver input	GS	05/27/04
P3.5	Adds Note 2	GS	02/04/05
P3.6	Added MIL-STD-202 test conditions (pg 2) / Corrected NAI naming convention: S1, S4 are Sin(-) and Cos(-) – respectively (pg.2)	FH/as	04/10/06
P3.7	Supplemented BIT/Wrap around specification descriptions (pg. 2); Re-format	FR/as	06/01/06
P3.8	Corrected front page photo;	as	06/02/06
P3.9	Corrected BIT, Protection, Reference output and Enclosure specifications. Added K & CO pins to B enclosure pin outs & added kick circuit note to B enclosure notes. Expanded Part number list to include B2 & B3 options for Metric captive hardware, annotated Mechanical drawing to show Metric hardware option. Corrected typos on pg 1 & 3.	FR	10/24/06
A	Corrected op. temp. range pg 3, moved Mechanical page to pg. 6, changed rev. designation to A Released.	FR	12/05/06
B	Modified P/N chart – Changed "A" & "B" to "A0" & "B0" for consistency.	FR	01/04/06
C	Additional changes to P/N definition. Added provision for special codes and for specifying 400 Hz Unit. Clarified ordering information for optional ref. transformer.	FR	01/04/06
D	Added option for kick circuit internal / external enable for B enclosures; reformatted P/N table consistent with other specs.	FR	02/03/07
E	Added options/clarifications for wrap output signals (pg. 3) and PCB conformal coat (added part number designator option codes K/0 (conformal coat) and 41, 61 (additional wrap phasing options).	AS	06/10/08
E1	Agile release / Added clarification note 1 in part number: Legacy part numbers without P/N digit for conformal coat to be identified as "No Conformal Coat".	AS	06/12/08
F	Corrected BIT operation (Pg. 4); Added BIT and ON/OFF connection diagrams (Pg. 5).	AS	11/25/08
G	Clarified part number – "A" enclosure does not provide "wrap" signals (wrap only applies to "B")	AS	03/17/09
H	Corrected Enclosure "A" base plate mechanical thru hole spacing from 4.590 to 4.700 and from .250 to .195 (pg. 7); Clarified REF transformer/kick circuit options in part number configurator (pg. 8).	FR/as	01/08/10
J	Clarified / Added P/N options RE: Wrap option, Corrected double entry in TOC.	FR	01/26/11
J1	Added mechanical options B4, B5	AS	08/08/12
J2	Clarified mechanical option(s) B4, B5 drawing (pg.7) – no baseplate hardware	AS	09/25/12
J3	ECO C02183: updated enclosure "B" drawing removing reference of PEM CLS-632-3 2 pls. from baseplate (0.0187 dia. thru hole 2 pls. only); revert and clarify (retract rev P3.6) 44PA1 resolver input SIN/COS (+/-) naming convention definition (back to rev. P3.3).	AS	11/25/13